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[Title of the Invention] MEMORY DEVICE HAVING AUTOMATIC DATA PROCESSING FUNCTION

[Claims]

[Claim 1] In multiple memory devices electrically connected to a Central Processing Unit (CPU) via a bus line, each of the memory devices includes;
storing means to store an individual code of the memory device itself,
fetching means to fetch a control instruction including an individual code, search instruction code, first and second address data, and a search data,
determining means to determine if an individual code in the control instruction fetched by the fetching means is identical with the individual code stored in said storing means,
comparator means to compare search data fetched by the fetching to stored data in a corresponding memory device,
search means to execute data search according to a control instruction code fetched by said fetching means by reading data stored in the corresponding memory device in the range specified sequentially by the first and the second address data and giving it to said comparator means, when said determining means determines identical,
control means not to execute the data search when the determining means determines not identical.

[Detailed Description of the Invention]

The present invention is related to a memory device having automatic data processing function electrically connected to a Central Processing Unit (CPU) via a bus line and executes internal processing according to a control instruction from the

CPU.

Traditionally, in a small computer system including program, for example, a memory device connected to a CPU via a bus line, RAM (Random Access Memory) for example, is address controlled directly by the CPU. That is, a data signal, a read/write signal, a chip enable signal, an address designation signal and so on are transmitted from the CPU via a bus line, communication of data between the RAM and the CPU is conducted according to those signals. In order to achieve that, all address lines for designating addresses of the RAM connect the CPU and the RAM. Therefore, if capacity of the RAM is increased, the number of the address lines has to be increased, then the number of lines has to be increased. Furthermore, when data in the RAM is searched or shifted, the CPU can not execute other processes, thereby the processing speed of the computer is decreased.

The present invention is conducted based on the problems above mentioned, and its purpose is to provide a memory device automatic data processing function which can perform a parallel processing with the CPU by executing data search with the memory device itself against a search instruction sent from the CPU.

Hereinafter, one embodiment of the present invention is explained with Fig.1 to Fig.4. Fig.1 is a schematic system construction drawing of a small computer to which a memory device according to the present invention is connected. In Fig.1, numeral 1 denotes a CPU and an operation key of the keyboard 2 is selected according to sampling signal output from the CPU, key input signal corresponding to the key operation is input to the CPU 1. CPU 1 transmits display data and the data is displayed on a display device 3. The CPU 1 connects a first RAM 4 and a second RAM 5 via a bus line BL as a memory device. The CPU 1 outputs predetermined clock pulse $\phi 1$, $\phi 2$, chip enable signal CE and operation signal OP to the first RAM 4 and the second RAM 5 respectively. The CPU 1 transmits 4-bit of data D1 to D4 between the first RAM 4 and the second RAM 4 and interrupt signal INT is transmitted to the CPU 1 from the first RAM 4 and the second RAM 5.

Fig.2 is a circuit drawing to show details of the first RAM 4 and the second RAM 5. In Fig.2, numeral 6 denotes a control circuit to which clock pulse $\phi 1$, $\phi 2$, chip enable signal CE and operation signal OP are transmitted from the CPU 1 respectively. Said control circuit 6 includes a latch 6a, a decoder 6b and a timing signal generation circuit 6c, and an instruction code among said data D1 to D4 is written in the latch 6a via the bus line gate 7. The instruction code in the latch 6a is decoded by the decoder 6b, and the output of it is transmitted to the timing generation circuit 6c. The timing generation circuit 6c creates and transmits timing

signal ϕA, ϕB, ϕC, R/W signal, signal CK1, CK2 and control instructions 01 to 07 based on the decode output from the decoder 6b and the clock pulses ϕ1, ϕ2. Open and close of said bus line gate 7 is controlled with said control instruction 07, and in the open state, data D1 to D4 are passed through to be input to the control circuit 6, and the first address counter 8, the second address counter 9, latch 10, 11, 12, and the I/O controller 13. Said latch 10 writes data indicating DEVICE NO among data D1 to D4 to be input at timing of said timing signal ϕC and transmits it to a device comparator 14. The device comparator 14 compares setting DEVICE NO supplied from a device setting part 15 to said DEVICE NO input from the latch 10, and when a result of the comparison is identical, outputs an identical signal to the control circuit 6. Said device setting part 15 comprises terminal V1 to V4, and it defines the DEVICE NO of the first RAM 4 as 4-bit data, for example. Said latch 11 latches search data and shift digit data among data D1 to D4 to be input at timing of the timing signal ϕA, and outputs the data to the data comparator 16 and an adder-subtracter circuit 17.

Each of said first address counter 8 and second address counter 9 has capacity of 12 bits, and designation of up or down, reset, and reading of address data among said data D1 to D4 of each address counter are controlled with corresponding said control instruction 01 and 02, and each conducts counting of corresponding signal CK1 and CH2, and counted address data is input to said adder-subtracter circuit 17 and it is transmitted to the address comparator 18 and the MAR circuit (Memory Address Recall circuit) 19. Input to the MAR circuit 19 is controlled with said control instruction 06, and one of address data of the first address counter 8 or the second address counter 9 is transmitted to the CPU 1 via the bus line gate 7 at every 4 bits. Said adder-subtracter circuit 17 is controlled with said control instruction 02, and transmits address data transmitted from the first address counter 8 or the second address counter 9, or adding-subtracting result of those address data and contents of the latch 11 as address data to the RAM 20, address data AD output from said adder-subtracter circuit 17 is also output to the address comparater 18. The address comparater 18 compares address data of the first address counter 8 to address data of the second address counter 9 when a signal from the interrupt controller 21 is "0", and when said signal is "1", address data of the first address counter 8 is compared to address data AD from the address comparater 18, when they agreed, identical signal is output to the interrupt controller 21. Data read from the RAM 20 via the I/O controller 13 is latched to said latch 12 at the timing of timing signal ϕB, the data is transmitted to the data

comparator 16. The data comparator 16 compares contents of the latch 11 to contents of the latch 12, and outputs the ide3ntical signal to the interrupt controller 21 when they agreed. The interrupter controller 21 is controlled with said control instruction 05 to output said "0", "1" signal, and outputs the interrupt signal INT to the CPU 1 and to the control circuit 6 when the identical signal is input. Said I/O controller 13 includes a 4-bit latch to latch data read from the RAM 20 and to transmit the data to the RAM 20 again according to said control instruction 04, or to output the latched data to the bus line gate 7, and also includes a circuit to clear contents of the RAM 20 with creating all "0" data. Said RAM 20 is designated to read state or write state with R~W signal, and executes write or read from/to the region corresponding to input address data.

Fig.3 shows an example of instruction types transmitted from the CPU 1 to the first RAM 4 and the second RAM 5 as 4-bit data of D1 to D4. In Fig.3A, whole instruction comprises 5 digits of X0 to X4, each has 4 bits, among them, DEVICE NO data designating the first RAM 4 or the second RAM 5 is transmitted to the digit X0, operation code OPE indicating a type of instruction is transmitted to the digit X1, RAM ADDRESS designating address data of the RAM 20 is transmitted to digit X2 to X4. When an instruction to read data in memory region from 2 initial addresses respectively designated by 2 addresses of the RAM 20 sequentially (called a binary instruction) is executed, as shown in Fig.3B, data for 5 digits of D1 to D4 as same as those of Fig.3A are output sequentially two times from the CPU 1. When a Shift instruction to shift up or down a designated address of the RAM 20 at predetermined digits is executed, or a Search instruction to search in a range from address 1 to address 2 in the RAM 20 and to read corresponding data is executed, as shown in Fig.3C, data D1 to D4 having 5 digits of digit X0 to X4, which is the same type as Fig.3B, are output two times, and the number of digits to be shifted as data for digit X1, X2, X3, or data to be searched are output sequentially.

Hereinafter, operation of the present invention is explained from a case that READ instruction is executed on the first RAM 4. As shown in Fig.4, clock pulse $\phi 1$, $\phi 2$ are kept outputting from the CPU 1. In this case, the operation signal OP and the chip enable signal CE are output from the CPU 1 respectively at the timing of signal $\phi 2$ trailing, as a result the first RAM 4 and the second RAM 5 start reading of instruction codes (instruction reading cycle). Next, data D1 to D4 of "1100" indicating DEVICE NO designating the first RAM 4 in the form shown in Fig.3A is output from the CPU 1 at the timing of clock pulse $\phi 1$ trailing. On the other hand, the control circuit 6 outputs the control signal O7 when both of the operation signal

OP and the chip enable signal CE are input, as a result, the bus line gate 7 is opened. Thereby, data of the DEVICE NO is written in the latch 10 at the timing of signal ϕC via the bus line gate 7. As the preset device NO data "1100" indicating the first RAM 4 is input to the device comparator 14 from the device setting part 15, the device comparator compares the data to contents of the latch 10, when they agrees, the identical signal is output to the control circuit 6. When the identical signal is output, the control circuit 6 writes X1 operation code OPE [0000] indicating the READ instruction after the DEVICE NO of X0 to the latch 6a. The operation code OPE written in the latch 6a is decoded by the decoder 6a, and the READ instruction is translated to start the READ process. That is, the control instruction 01 is output from the control circuit 6, after the operation code OPE of the X1, RAM ADDRESS of X2, X3, X4 output from the CPU 1 sequentially are set to the first address counter 8 sequentially. Like this, instruction code of the X0~X4 are set to the first RAM 4, after the setting, output of the operation signal OP, the chip enable signal CE have been kept outputting from the CPU 1 are stopped at the timing of clock pulse 01. Next, when the chip enable signal CE is out put from the CPU 1 while the operation signal OP is stopped, the data process cycle starts, and then the control circuit 6 starts the READ operation of RAM 20 according to the operation code OPE written in the latch 6a. That is, the initial address of the RAM 20 is designated via the adder-subtracter circuit 7 according to contents of the RAM ADDRESS set in the first address counter; furthermore R/W signal input to the RAM 20 becomes to be "0". Thereby, RAM DATA in the designated address of the RAM 20 is read out to transmit to the CPU 1 via the I/O controller 13 and the bus line gate 7 respectively. Next, the signal CK1 is output from the control circuit 6, the first address counter 8 is count upped by the signal CK1, the next address of the RAM 20 is designated with the address data to read out the next RAM DATA.

Similarly, each output of the signal CK1, contents of the first address counter 8 is incremented to execute reading of the RAMDATA. When output of the chip enable signal CE from the CPU 1 is stopped, output of the signal CK1 is also stopped to end the READ operation.

Next, an operation when a binary instruction of Fig.3B is output from the CPU 1 is explained. In this case, each data of digit X0~X4, DEVICE NO, OPE, RAM, ADDRESS 1, are input via the bus line gate 7, the DEVICE NO is input to the latch 10, the OPE is written in the latch 6a, and decoded to be a binary instruction in the control circuit 6. The input RAM ADDRESS, for example "50", is set to the first address counter 8. Similarly, the OPE RAM ADDRESS output from the CPU 1 at

the second time, for example “100”, is set to the latch 6a and the second address counter 9. Thereby, the second address counter 9 in incremented at +1 from the address “100” according to the control signal O2 and the signal CK2, the first address counter 8 is incremented at -1 from the address “50” according to the control signal O1 and the signal CK1. Incrementing the address at “+1” or “-1” is determined by contents of operation code OPE1 and OPE2. The control circuit 6 designates address of the RAM 20 according to contents of the first address counter 8 when the chip enable signal CE output from the CPU 1 changes from “0” to “1”, and designates address of the RAM 20 according to contents of the second address counter 9 when the chip enable signal CE output from the CPU 1 changes from “0” to “1” again. Data read from the RAM 20 is transmitted to the CPU 1 via the I/O controller 13 and the bus line gate 7. The CPU 1 changes the chip enable signal CE “0” or “1” alternately to read out data of the address designated by the first address counter 8 or the second address counter 9.

Next, a case that the Search instruction of Fig.3C described above is output from the CPU 1 is explained. In this case, OPE1 and OPE2 among data X0~X4 output from the CPU 1 are written in the latch 6a respectively, RAM ADDRESS 1, “50” for example, is set to the first address counter 8 and RAM ADDRESS 2, for example “100”, is set to the second address counter 9, and the Search data, for example “AAA”, is written in the latch 11. Count contents of the address counter 8 is incremented at “+1”, at each time, RAM DATA in corresponding address of the RAM 20 is read out to be written to the latch 12 via the I/O controller 13. Contents of the latch 12 and contents of the latch 11 are compared by the data comparator 16; when the comparison result is not agreed, the first address counter is incremented at “+1” and compared RAM DATA latched in the latch 12 again. When the result is agreed, the identical signal is output to the interrupt controller 21, and the interrupt controller 21 outputs the interrupt signal INT indicating end of Search operation to the CPU 1 and the control circuit 6. At the same time, contents of the address counter 8 indicating address of the searched RAM DATA “AAA” is transmitted to the CPU 1 via the MAR circuit 19 and the bus line gate 7. Contents of the second address counter 9 and contents of the first address counter 8 are compared by the address comparator 18, and when RAM DATA “AAA” are not searched in the RAM 20, and contents of the first address counter is “100”, the identical signal is output to the interrupt controller 21, as a result, the interrupt signal INT is transmitted.

Though the structure the first RAM 4 and the second RAM 5 are fixedly placed in a small computer in the embodiment above mentioned, the present invention is not

limited to this, the structure may have cassette type of the first RAM 4 and the second RAM 5 detachably connected to the CPU 1. Furthermore, though RAM is used as memory in the embodiment above mentioned, the present invention is not limited to this, ROM (Read Only Memory) may be used. The present invention is not limited to a small computer; it may be applied for other electronic devices.

As mentioned above, in the present invention, as the CPU transmits the individual code designating one memory device, control instruction including the first and the second address data and the search data, and the memory device determines whether the received individual code agrees its own code, and when they agreed, it reads out memory data in the range indicated with the first and the second address data to execute data search with comparing received search data, data amount to be handled becomes smaller, even when plural of memory devices are used, as the CPU can instruct each memory device to execute search operation in specified range after outputting the control instruction, the CPU can execute other processes in parallel, the processing speed of the whole system can be increased.

[Brief Description of the Drawings]

Fig.1 is a schematic system construction drawing using one embodiment of the present invention.

Fig.2 is a circuit structure drawing to show details of the first and the second RAM.

Fig.3A, B, C are drawings to show instruction types.

Fig.4 is a time chart to explain the operation.

1...CPU

4...First RAM

5...Second RAM

6...Control circuit

8...First address counter

9...Second address counter

17...Adder-subtractor circuit

20...RAM

Fig.4

Fig.1

1. CPU
2. Keyboard
3. Display device
4. First RAM
5. Second RAM

Fig.3

Fig.2

6a Timing signal generation circuit

6b Decoder

6c Latch

14 Device comparator

10 Latch

7 Bus line gate

8 First address counter

9 Second address counter

11 Latch

18 Address comparator

16 Data comparator

21 Interrupt controller

12 Latch

17 Adder-subtractor

13 I/O controller